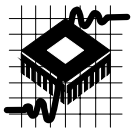
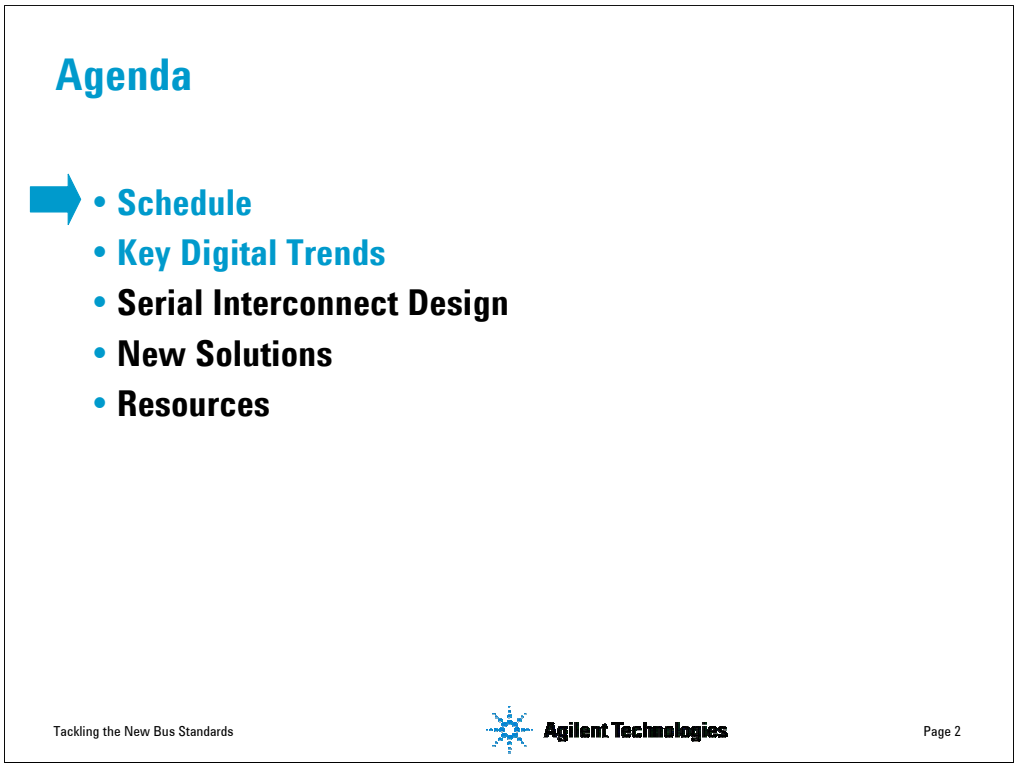
Tackling the New Bus Standards – Today and Tomorrow



Agilent Technologies

Welcome to the Tackling Today's High-Speed Serial Interconnects high-speed digital design seminar.



Our agenda for this presentation is to review the key digital trends, the basics of serial interconnect design/test, new solutions, and some helpful resources.

Schedule

Time	Session
9:15 am	Tackling the New Bus Standards
10:00 am	SI Measurements of High-Speed Differential Channels
11:00 am	PCI Express Electrical Characterization and Compliance
12:00 pm	Lunch/Product Fair
1:00 pm	Jitter Characterization and Measurements
2:00 pm	PCI Express Protocol Analysis, Debug and Compliance
3:00 pm	Practical Probing Techniques with Scopes and Logic Analyzers
4:00 pm	Wrap Up/Q&A/Product Fair

Here is the how the day breaks down. After this introductory lecture, we have five 60 minute lectures, two before lunch, 3 after.

Key Digital Trends

- **Increasing Integration** – ***FPGA Centric Designs***
- **Increasing Speed** – ***Signal Integrity Issues***
- **Architectural Shifts** – ***High Speed Serial Interconnects***

Tools and techniques need to keep pace ...

RapidIO

HyperTransport CONSORTIUM

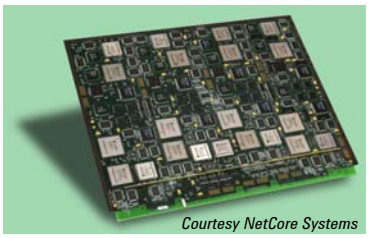
PCI EXPRESS

I think it's important to review the key digital trends impacting designers today to put the labs you'll go through into perspective. In the applications of digital technology, it seems that we can find three major trends that impact digital design today – increasing integration, increasing speed, and architectural shifts. We'll look at each area a bit more in-depth. Fundamentally, the rate of change in technology is forcing design and test tools to evolve just as fast. Have your tools and techniques kept pace?

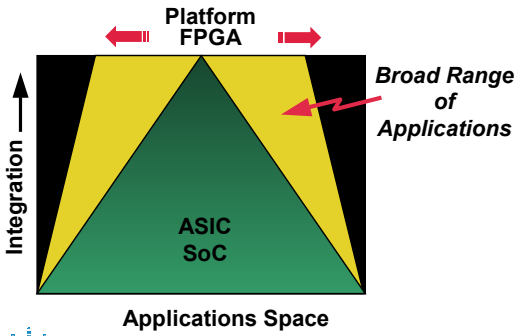
Increasing Integration

- **High use of ASICs & FPGAs**
  - **Mfg. Cost vs. Time-to-Market (ASIC vs. FPGA)**
  - **FPGAs offer easy upgrade path, are standard parts, quick to market**
  - **>1M gates, >100 MHz, >3M BRAM, ...**
  - **Serial I/O up to 10 Gb/s**
  - **H/W and S/W integration**

How do I see what's happening inside? ... new Logic Analyzer tools



Courtesy NetCore Systems



Of course this integration has gone hand-in-hand with the continual improvements in ASIC and FPGA technology. It used to be that ASICs were the vehicle to drive down the cost of a product since they're inexpensive in volume, but they take a long time to design. Now we have FPGAs that rival ASICs in functionality – >1M gates, >100 MHz operation, >3M BRAM (bank memory) – plus the ability to easily create the design. The benefits are now a shorter time-to-market and the ability to change the "glue" quickly to adapt to product changes, albeit at the expense of a higher manufacturing cost.

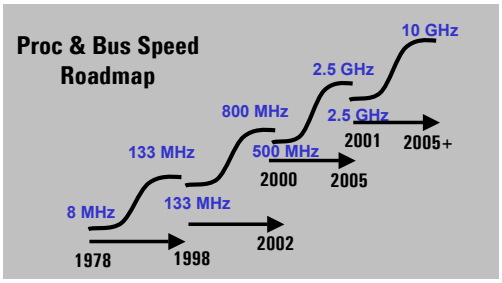
Upfront design costs vs. manufacturing costs – ASICs and FPGAs definitely differ here. But as this graphic shows, with the increased capability of FPGAs they are finding a broader range of applications. And as FPGA capacity grows, users are demanding better EDA tools. High volume products will always benefit from using ASICs, but FPGAs are making impressive inroads.

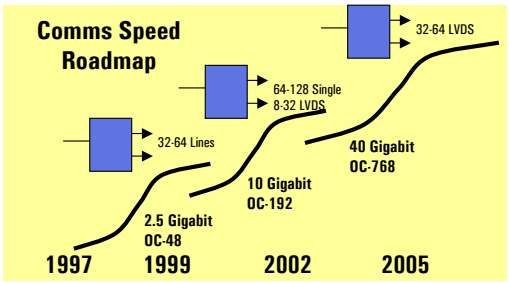
The challenge of so much circuitry being placed in an ASIC or FPGA is in debugging what's happening when things don't work right. Before the discrete parts on the board could be easily probed, now it's all inside the chip. How do I see what's going on inside the chip?

Increasing Speed

- **Signal Integrity Issues**
  - **Clock Speeds >2 GHz**
  - **Edge Rates <1 ns**
  - **Crosstalk, Impedance, EMI, and Jitter measurements**
  - **Channel modeling is required**

I'm becoming a microwave designer!





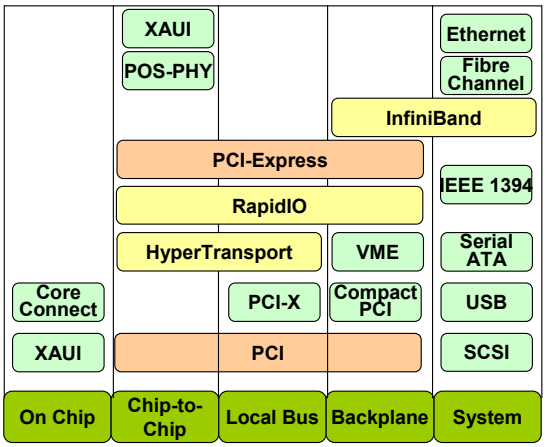
A closer look at the performance drivers in the PC and Communications markets shows many similarities. The technology "waves" bring new CPU speeds and bus speeds. With clock speeds breaking 2 GHz today and edge rates below 1 ns, what happens on-board or on-chip is better accounted for using RF/Microwave theory for digital design, what we tend to call Signal Integrity problems. While what clock frequency, edge rate, or bandwidths seem to bring on SI issues are debatable, the effects are always the same. A square-wave or pulse rarely look square with ringing and overshoot. The multiple bus lines now show coupling effects that we measure as crosstalk and reflections. You have to pay special attention to bus layout and terminations to minimize EMI. With the sophisticated bus protocols being developed, jitter is a growing concern. It seems that the Signal Integrity engineer is really doing RF/Microwave design but without the specialized tools an RF engineer would use. Traces are no longer just connections between ICs but rather a potential signal degrader. How do I learn the RF techniques without having to be an RF engineer?

I like to think of SI this way. You buy a fancy sports car because want to drive fast and get the most out of it. But if the streets in your city are full of potholes, you can't drive very fast so you build a freeway to speed. Envision the next digital bus with higher data rates as trying to build the fastest freeway so that your data can speed along. Building a better channel is the goal!

Architectural Shifts

- **Fast/Wide Parallel to Fast/Differential Serial**
  - **Layout, EMI and Skew tradeoffs**
  - **Point-to-point networks**
  - **>1 Gb/s data rates**
  - **Compliance tests**
  - **Design knowledge of differential signals**

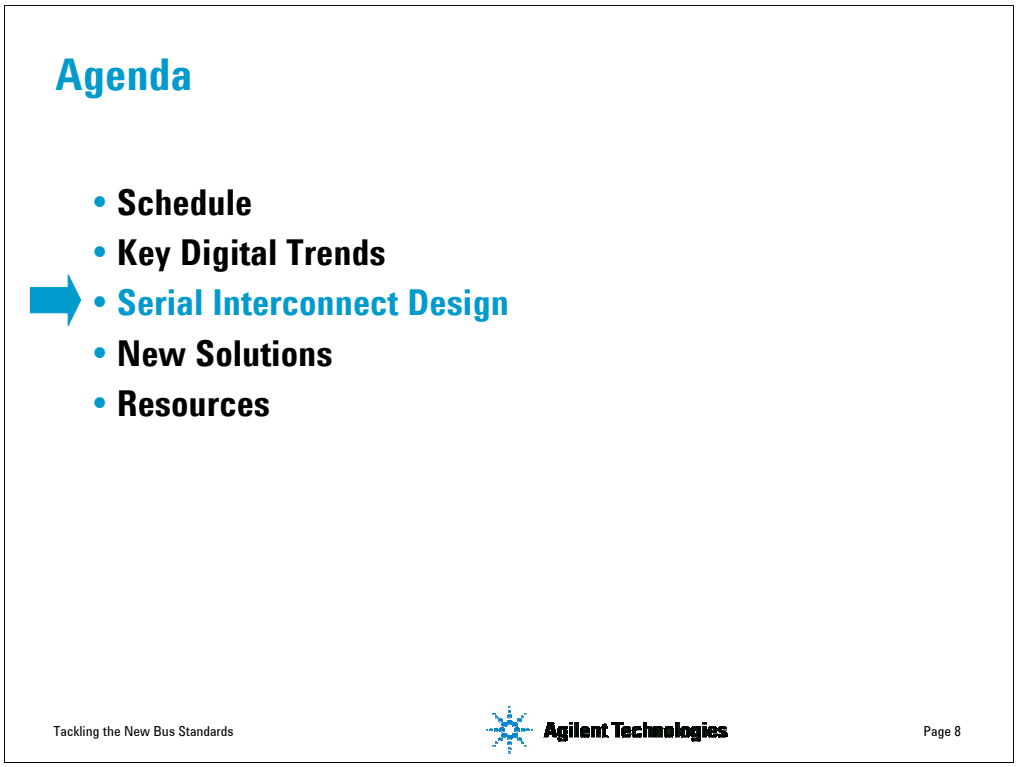
How do I probe the signals?



The third major trend is that of architectural shifts, both in how we design and how teams operate. We mentioned the growing number of high-speed buses being developed to improve throughput. This graphic illustrates how many of these new bus standards are likely to be applied – on-chip, between chips, on-board, backplane, or in a system. The knowledge and design intent of the system oriented buses have definitely migrated to the board and on-chip solutions as the volume of data and level of data abstraction has increased.

Most new buses today attempt to overcome some fundamental problems of existing buses by using fast/differential serial approaches as opposed to fast/wide parallel designs. While the fast/wide parallel approach provides the fastest data transfer, inherent in this approach are significant layout, EMI, and skew problems. Besides, there is a realistic limitation on how wide a parallel bus you want. Thus we're challenged to understand the shift from single-ended to differential design. It's not the same as two parallel traces, plus how you probe the bus is more difficult.

The system buses have also brought the point-to-point networking concept to the new on-board and on-chip buses. The point-to-point approach allows more modularity, increases the level of abstraction via the protocols used, and forces a compliance test to ensure components, modules, and subsystems meet the spec. We now see Plug Fests happening to help designers ensure compatibility or to better understand why they're not. Taming the bus on your board is now much more complicated as the data becomes encoded. How do you inspect the data at multiple levels of abstraction so that you can truly debug a design?



Now let's review the basics of serial interconnect design.

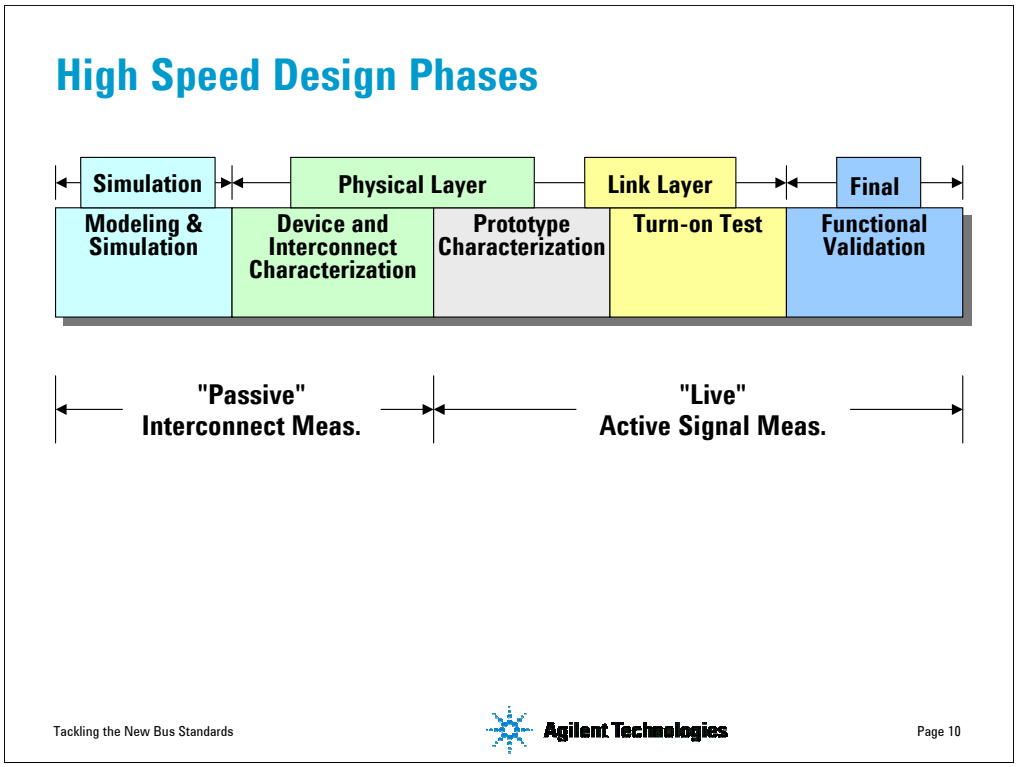
Bandwidth Requirements for New Standards

Serial Bus Standard	Embedded Clock Rate	Fundamental Frequency of Data Signal	3rd Harmonic Frequency of Data Signal	5th Harmonic Frequency of Data Signal
PCI Express I	2.5 Gb/s	1.25 GHz	3.75 GHz	6.25 GHz
SATA II	3.0 Gb/s	1.5 GHz	4.5 GHz	7.5 GHz
XAUI	3.125 Gb/s	1.56 GHz	4.69 GHz	7.81 GHz
Fibre Channel	4.25 Gb/s	2.125 GHz	6.375 GHz	10.625 GHz
FBD	4.8 Gb/s	2.4 GHz	7.2 GHz	12.0 GHz
PCI Express II	5.0 Gb/s	2.5 GHz	7.5 GHz	12.5 GHz
SATA III	6.0 Gb/s	3.0 GHz	9.0 GHz	15.0 GHz
CEI	6.25 Gb/s	3.125 GHz	9.375 GHz	15.625 GHz
Proprietary	7.0 Gb/s	3.5 GHz	10.5 GHz	17.5 GHz

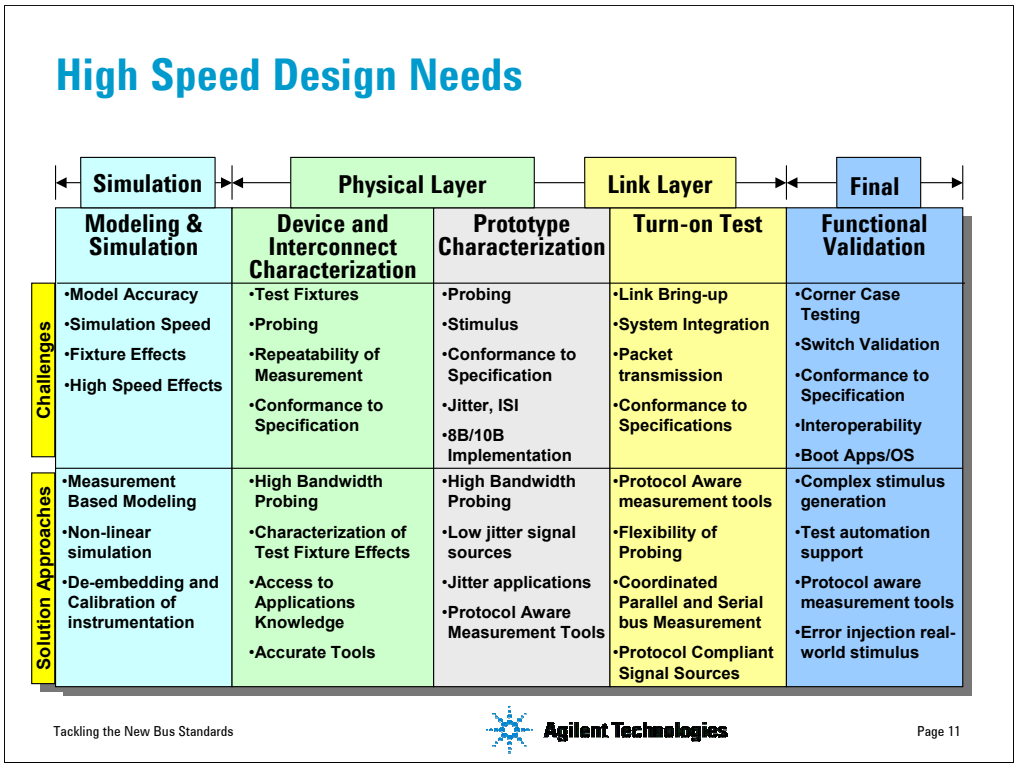
- New standards require higher BW measurement capability and analysis tools
- Probing, channel analysis and modeling will be critical for success

Here's a list of all the present and upcoming standards. When we think about the necessary measurements we need to make, it's important to recognize the necessary measurement bandwidth that will be required. Listed here are the standard, it's data rate, the actual frequency of the data signal (half the speed of the embedded/derived clock rate), and the frequencies of the third and fifth harmonics. We must remember that a square wave is composed of the fundamental and its' odd harmonics. A significant amount of the signal content exists at the third and fith harmonics of fundamental data signal frequency, so to properly characterize an eye diagram, rise/fall times, etc., our measurement solution needs the bandwidth to measure these. Of course, measuring just the fundamental or fundamental and third harmonic can give us a good idea of performance, the fifth is really required for reasonable validation.

We can see that a 6 GHz scope is barely satisfactory for PCI Express today, and that all the major new standards (or next generation ones) really will need 10-12 GHz of bandwidth! At these frequencies, probing will be a big issue. Likewise, the analysis and modeling of the interconnect channel will be very important.

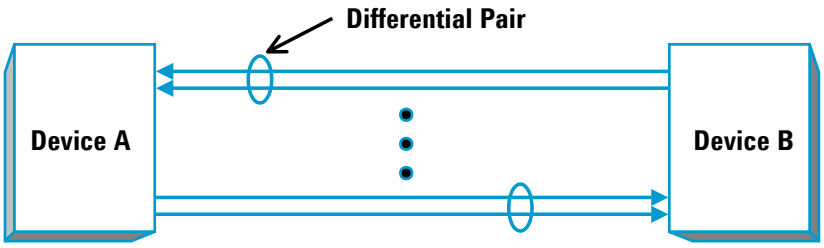


From Simulation to final functional design, new challenges are faced by the digital designer. Projects tend to have two distinct phases: a passive interconnect phase, and an active signal test phase. The better job we do in the passive interconnect design, the fewer problems we encounter in the active signal test phase.



If we look deeper into what challenges and measurement solutions are required for each of the five phases, we see that Signal Integrity, probing of high speed serial signals, conformance to standards, and interoperability are major challenges. You need the right equipment and measurement expertise to get product to market quickly.

Typical Serial Interconnect Electrical Design



- **Design:**
  - Point-to-Point Network Topology
  - LVDS (Low Voltage Differential Signaling) Technology
  - ≥ 1 Gb/s per Lane/direction
  - Potential Spread Spectrum Clocking (SSC)
- **Problem Areas:**
  - Crosstalk
  - Impedance Discontinuities
  - Reflections
  - InterSymbol Interference
  - Mode Conversion

Let's look at a typical high-speed serial interconnect. High-speed serial links can suffer from a large array of physical phenomena including crosstalk, impedance discontinuities resulting in reflections (causing jitter), intersymbol interference, and mode conversion due to unbalanced transmission lines can lead to excessive EMI emissions in a large system. Signal Integrity is all about optimizing signal transmission, in this case the serial interconnect/channel. I like to think of the channel as being a freeway – the more potholes it has, the slower you must drive.

Interconnect Characterization is Required

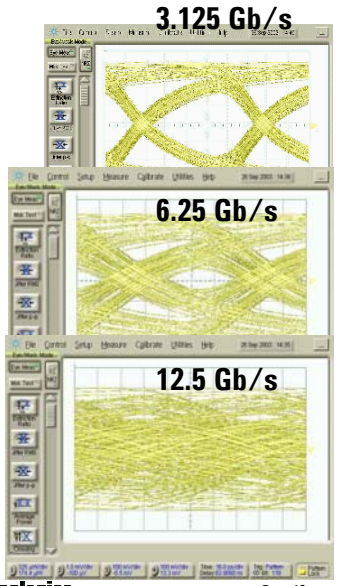
- Likely designing on FR4
- It's low cost and easy to manufacture
- BUT it has problems:
  - Reflections at high speeds
  - Dispersion
  - Insertion Loss
  - Frequency response
  - Jitter
  - Closed eyes

Need RF oriented tools for channel design

XAUI, 4G Fibre Channel

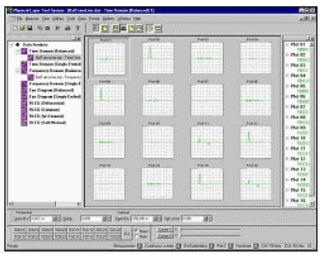
Back planes, 5-6G

Back planes, 10-12G



Once you build that better freeway, how fast can you pass data on it? Most designs are based on using FR4 since it's low cost and easy to manufacture, but it has insertion loss that increases with frequency. The measurements on the right here illustrate what that does to our data. On the top is an eye diagram for for backplane driven at 3.125 Gb/s. It looks ok. In the middle, we double the data rate to 6.25 Gb/s. The eye is starting to close both in amplitude and in time, here jitter is an increasing problem. Interestingly, the 5-6 Gb/s range is where most standards want to go next, and it's the next likely data rate for backplanes. On the bottom, we double the data rate again to 12.5 Gb/s and the eye is nearly closed. We have a non-functional system here. The industry has set its sights on the 10-12 Gb/s data range for next generation backplanes, so something has to change to make this work. So they're investigating pre-emphasis and equalization techniques that boost the signal level to compensate for the insertion loss and then try to correct for it. It's pretty similar to the Dolby B noise reduction approach for cassettes and digital audio – pump up the high-frequency components that get attenuated.

Interconnect/Channel Characterization



Physical Layer Test System (PLTS)

- Complete characterization of your device with one tool
- Works with both a VNA or TDR scope
- Unparalleled accuracy delivers confidence in measurements
- Superb for creating models for simulations
- Save time by measuring multiple parameters with one setup
  - Insertion Loss (S_{DD21})
  - Return Loss
  - Mode Conversion (S_{CD11}, S_{CD21})
  - Differential Trace Impedance (S_{DD11})
  - Data dependent jitter
- Also can measure Crosstalk (FEXT, NEXT)

The PLTS Software tool can be used with a TDR or VNA to provide the highest level of accuracy when characterizing or modeling transmission lines in a PCB, Cable, or connector. It offers unique capabilities in analyzing a differential channel and has links to common modeling tools so that you can refine your design.

Device Characterization: Transmitters

Measurement	54855A 7 GHz Real Time Oscilloscope w/SDA*	86100C DCA-J Sampling Oscilloscope w/TDR*
Unit Interval	●	●
Differential Voltage	●	●
Eye Diagram/Mask	●	●
Jitter	●	●
Rise/Fall Times		●
Common Mode Voltage	●	●
Idle Transition Time	●	●
Return Loss		●
Impedance		●
Lane Skew	●	●

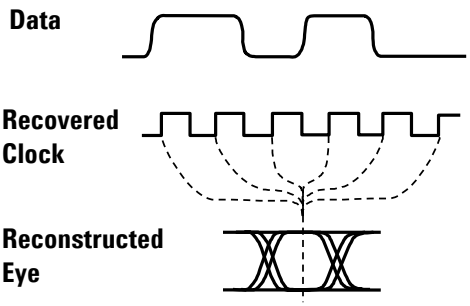
* Capability will vary by Standard

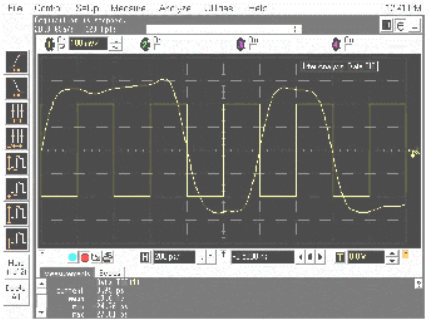
To fully characterize a Transmitter, both a real-time and a sampling scope are needed. The table lists all the measurements needed, based upon the PCI Express specification. Depending upon the bus standard, either the real-time scope or the sampling scope may be preferred for specific measurements.

For PCI Express 1.0a, most specification are required to be measured over 250 consecutive UI (unit intervals), and therefore require a real time scope with serial data analysis capability. A sampling scope does not measure consecutive UIs. However, the risetime specification is too fast for real time scopes available today, so a sampling scope must be used. The sampling scope provides TDR capability which is used tom measure the impedance. Return loss can be measured with a TDR and PLTS software, or alternatively, a VNA can be used.

For the most accurate measurements, a direct connection from the transmitter's TX output to the scope inputs should be used. This offer the lowest noise measurement. If a direct connection is not possible, then a differential prove proves good performance also, but adds a small amount of noise and jitter to the measurement. In the case of the risetime, impedance, and return loss measurements, a direction connection is required.

Serial Data Means Reconstructing the Eye





- Can use Hardware or Software clock recovery
- Embedded clock not always obvious from the data waveform
- 8b/10b Encoding is typically used

The key to making measurements is that we need to extract the embedded clock from the data. We can recover the clock either by hardware clock recovery, or in software. There are advantages and disadvantages to both approaches. Software clock recovery requires no extra hardware and can be configured to mimic the loop bandwidth of hardware colock recovery.

For software clock recovery, the scope examines the captured data to calculate the optimal clock instants. From this is generates a “recovered clock.” Keep in mind the “recovered clock” is not a “real” signal operating .

Having generated a recovered clock, the scope then folds the data on itself using the recovered clock to align the individual bit intervals. What you see on the screen looks just like the conventional eye diagram derived by triggering the scope on an external clock. But there are some significant advantages to doing it this way.

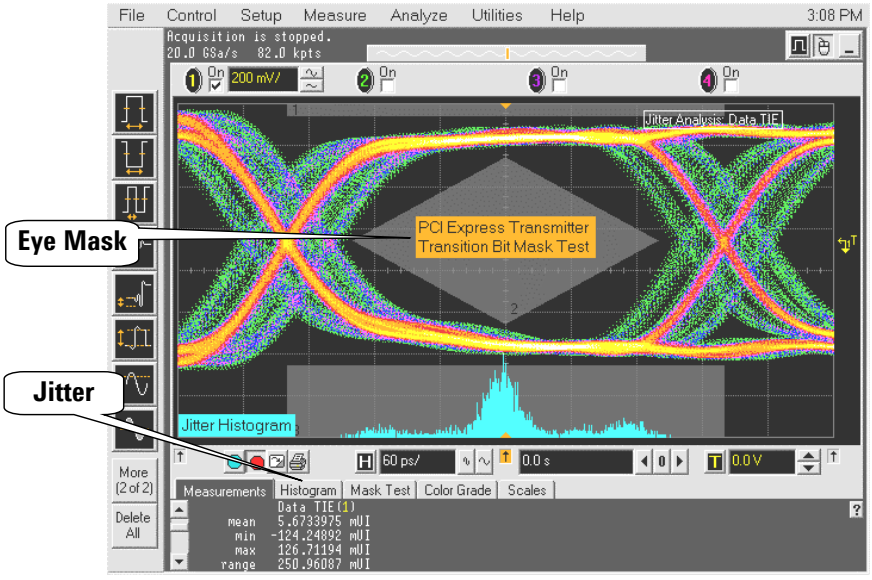
The actual throughput of bit intervals measured is much higher, even though the scope may appear to slow down in drawing the eye, especially for very deep memory (on the order of 1 M samples). That is because the scope is acquiring and displaying thousands of individual bit intervals on each acquisition. On a conventional eye measurement, you are limited to the eye at the center of the screen near the trigger point. This thus contains only one bit interval per trigger.

With software clock recovery, many bit intervals in sequence are captured. Thus, effects of ISI are clearly seen, and can be traced back directly to the causal sequences in the PRBS or other data pattern.

Trigger jitter and false triggers in the scope do not contribute to measurement error with this method. You could let the scope free-run with no trigger at all and it would not affect the results. The time of each bit interval is calculated relative to the recovered clock, independent of when or whether the scope triggered.

In the following examples we'll be using an Agilent 54855A Infiniium 6 GHz real-time scope. It has a sampling rate of 20 GSa/s on each of its four channels. The E2688A high-speed serial data analysis software application package is used to recover the clock. In this display, the clock and signal are overlaid in the same graticule. You can see that it isn't obvious where the clock edges were from the measured data signal.

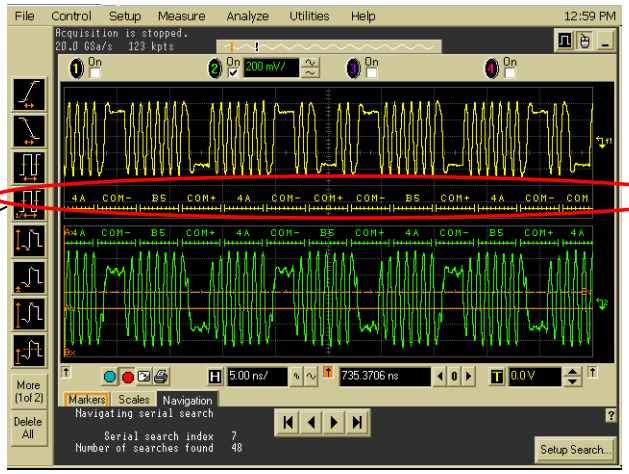
Transmitter Transition Bit Eye & Jitter Testing



Here is an example of a PCI Express eye and jitter measurement on a transmitter transition bit. Notice on the eyes after a transition bit are being measured. The color graded display give statistical information on the signals noise and jitter. The eye mask and jitter measurement are made over 250 consecutive UIs. Multiple acquisitions can be made to find worst case eye and jitter over multiple sets of 250 consecutive UIs. Mask test failures can be logged, and used to generate email notifications. The jitter histogram can be displayed for diagnostic information.

Validating 8b/10b Decoding

Designer must now also validate encoding and decoding algorithms



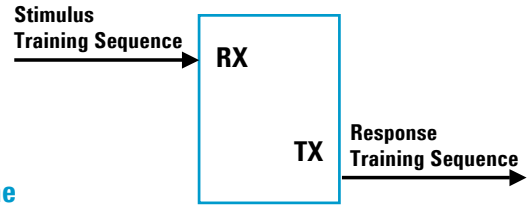
Symbol codes

B5 COM+ 4A COM-

Disparity

Since many of the standard utilize 8b/10b decoding to maintain data integrity, the designer now needs to validate their encoding/decoding algorithms so that the protocol designer can do their job. With 8b/10b, an 8 bit data signal gets 2 extra bits to form a unique symbol. If we look at the signal, it is a repetitive sequence of COM, 4A, COM, B5. This is the PCI Express search pattern to initiate contact with another PCI Express device. You can see that decoding lets the electrical designer validate that their circuitry is producing the right symbol.

Device Characterization: Receivers



A signal generator is used to stimulate the receiver, and the response of the device is monitored.

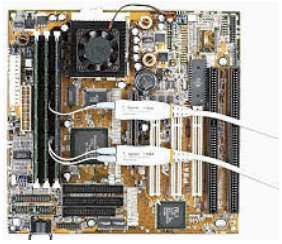
- **Most testing can be performed with an 81134A Pulse Pattern Generator and a function generator as the stimulus source.**
- **An oscilloscope and probe are used to monitor the signal into the receiver.**
- **An oscilloscope or logic analyzer is used to monitor the response from the device.**
- **Receiver input impedance and return loss is measured with a TDR or VNA.**

Receivers must be tested for the sensitivity, and tolerance to jitter. The testing methodology is to provide a stimulus to the RX input of a device, and monitor the response from the device via the TX pins. Note that this testing methodology assumes that the device's is functional enough to response correctly to Training Set inputs on it's RX inputs. An signal generator such as the Agilent 81134A is ideally suited for most tests, the exception being lane to lane skew tests. A function generator is used to add jitter to the stimulus signal. The signal should be monitored at the device's input pins with an oscilloscope and probe, to know what the actual signal amplitude and jitter is AT the device's input. The response from the device can be monitored with an oscilloscope or logic analyzer. In additional to sensitivity and jitter tolerance, the receiver's input impedance and return loss must be measured with a TDR or VNA.

Active Probing Impacts Accuracy & Bandwidth

In a Perfect World ...

- **Probes don't load your circuit**
- **Probes accurately reproduce signals at the probe tip with high fidelity**



Realities in the Real World ...

- **Probes have traditionally been the "weak link" in the measurement chain when making high bandwidth signal integrity measurements**
- **All probes will load the circuit under test to some degree**
- **Probing accessories can degrade performance significantly**

Tackling the New Bus Standards

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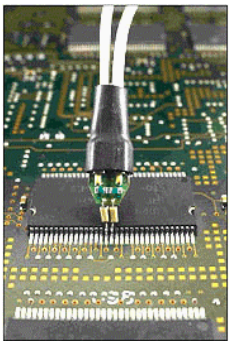
In a perfect world, probes don't load your circuit, and they accurately reproduce your signals under test. However in the real world, probes have traditionally been the "weak link" in the oscilloscope measurement chain for high-speed applications. All probes will load the circuit under test to some degree. So the goal with high-speed active probing is to minimize circuit loading. In addition, probing accessories are usually the primary culprit in limiting performance of measurements.

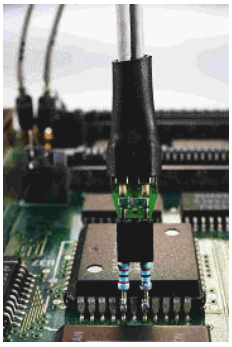
The key to achieving minimal loading and accurate reproduction of high-speed signals is short connections. Agilent's InfiniiMax differential active probes have been designed with a unique probe head technology that minimizes the length of connection for various use-models. In today's hands-on probing lab, you will get an opportunity to use the various probe heads and observe the performance of each.

Signal Fidelity Begins at the Probe Tip

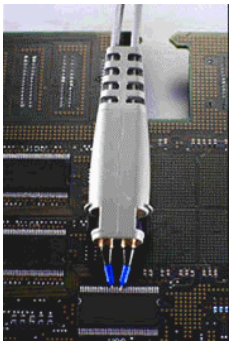
Minimize lead inductance and capacitance with flexibility for difficult access



- 10 cm solder-in
- 7 GHz differential
- 50 kΩ



- 10 cm socketed
- 7 GHz differential
- 50 kΩ



- Variable spacing browser
- 6 GHz differential
- 50 kΩ

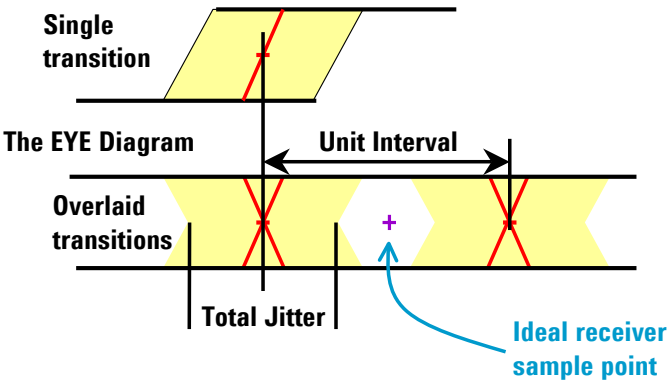
- SMA
- 7 GHz differential
- 100 Ω

Since signal fidelity begins at the probe tip, you want to be using a probe with minimal lead inductance and capacitance, plus have it be flexible enough to measure on DIMMs and other tight spots. Agilent's InfiniiMax probing system has a variety of probe heads optimized specifically for different probing use-models, including browsing, solder-in, socketed, and SMA connections. In addition, Agilent provides both differential and single-ended probe heads. However, it should be pointed out that differential probe heads can be used for both differential and single-ended measurements, and provide for a higher performance measurement including higher common-mode rejection and higher bandwidth.

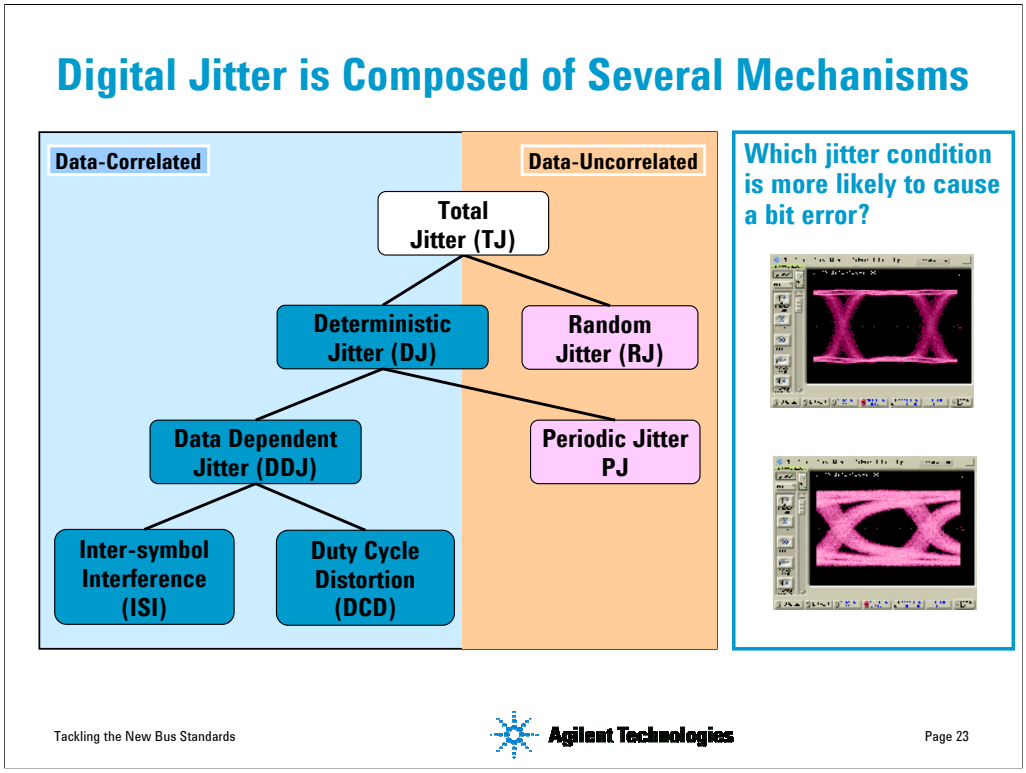
High Data Rates Mean Measuring Jitter

What is Jitter?

- **The deviation of a signal edge time at a defined amplitude of the signal from a reference time.**



We mentioned that with higher data rates the key timing specification is now jitter. Each standard approaches it differently, but it's important to realize how we look at jitter in digital systems. To review, jitter is basically the timing variation in an edge over time, commonly called the Time Interval Error, or TIE. We measure this typically via the eye diagram where multiple transitions are overlaid to form the eye. Total Jitter is specified to be the peak-to-peak maximum timing error.

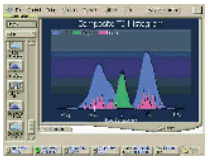


The jitter family tree is composed of a random, non-systematic contribution and a deterministic, systematic contribution. We can also distinguish between a data-correlated component and a data-uncorrelated component. In most cases, the random component is difficult to modify while we can change our circuits to impact the deterministic component. For most standards, the key specification is Total Jitter. Others also specify a random and deterministic jitter level. So measuring jitter will become very important for our customers.

So as a quick test, let's compare the two eye diagrams here to the right. Which of these two would you expect to have the most jitter and cause a bit error? If you think it's the bottom one, you would be wrong. While it appears to have more noise, it ends up that if you let the top measurement run a long time that the random component is actually larger and impacts the total jitter more. Remember that random jitter requires a peak-to-peak measurement over a statistically valid sample period. Typically we can't wait that long so we measure a shorter period and extrapolate the peak-to-peak value. Thus, it's important to really make a RJ/DJ measurement to quantify our RJ component.

Know Your Jitter

54855A Real Time Oscilloscope



86100C DCA-J Sampling Oscilloscope

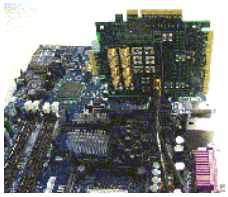
N4901 Serial BERT

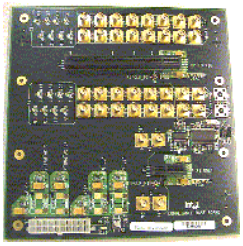
81250 ParBERT

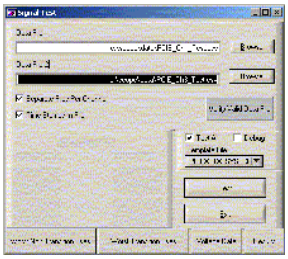
- **Jitter is specified and measured differently for each standard**
- **There are many views of jitter:**
  - Histogram
  - Bathtub curve
  - Spectrum
  - Total Jitter
  - RJ/DJ separation
  - DJ decomposition (ISI, ...)
  - ...
- **Select the optimum tool for your measurement**

A key measurement for high data rates is jitter. The are 3 different techniques for measuring jitter – a real-time oscilloscope, the DCA, and a BERT. Agilent offers a wide range of solutions when our competitors primarily offer only an oscilloscope. It's important to understand how the different measurement approaches differ, and what their strengths and weaknesses are. Many users are still learning how to measure jitter.

Compliance Tools Facilitate Adoption





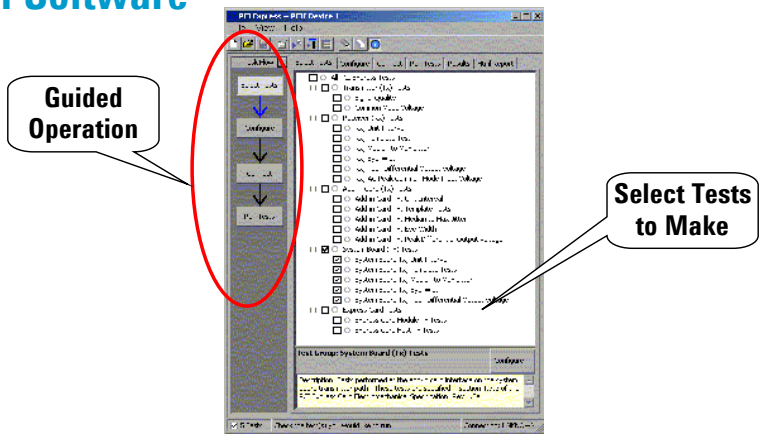


PCI Express Electrical Compliance Fixtures & Software

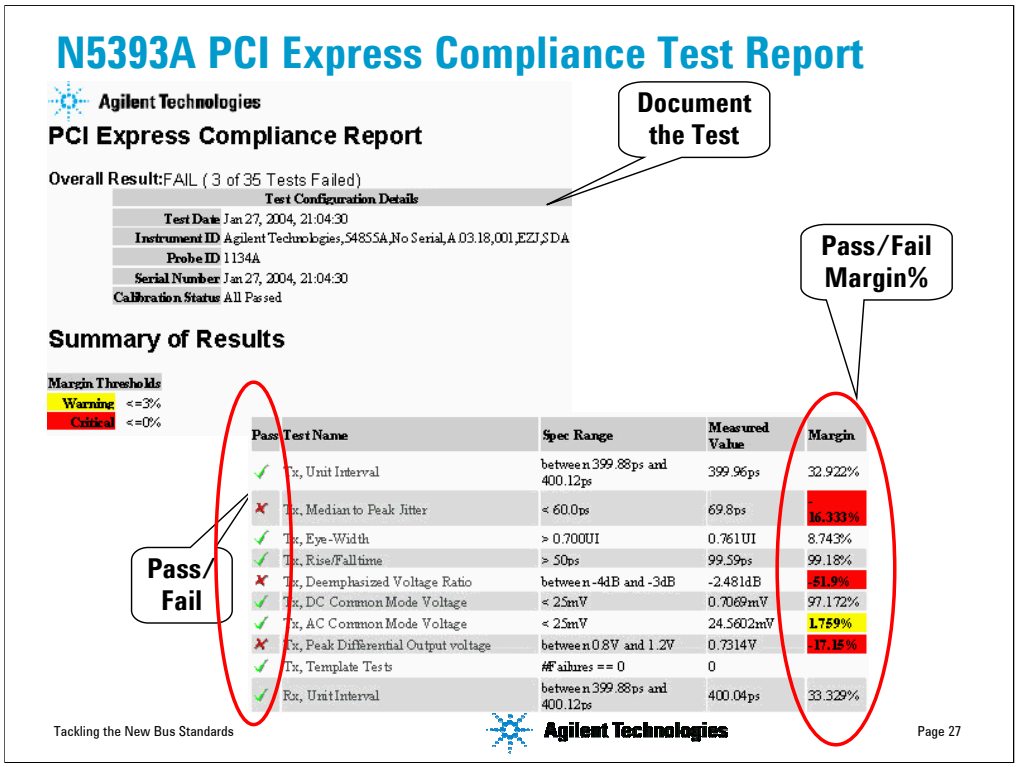
PCI Express Protocol Analyzer & Compliance Test Card

Compliance is necessary to ensure products are interoperable. Nobody wants to buy a hot new graphics card from ATI only to find out that it doesn't work in their Intel motherboard. So standards bodies typically offer for sale compliance fixtures to test add-in card or motherboards. Compliance test software for the electrical PHY layer and protocol analysis software for Data/Link layer are also required. Here are some examples for PCI Express – the compliance load board (CLB) for motherboards, the compliance base board (CBB) for add-in cards, and the SigTest software. Agilent has co-developed with Intel a low cost PCI Express Protocol Test Card.

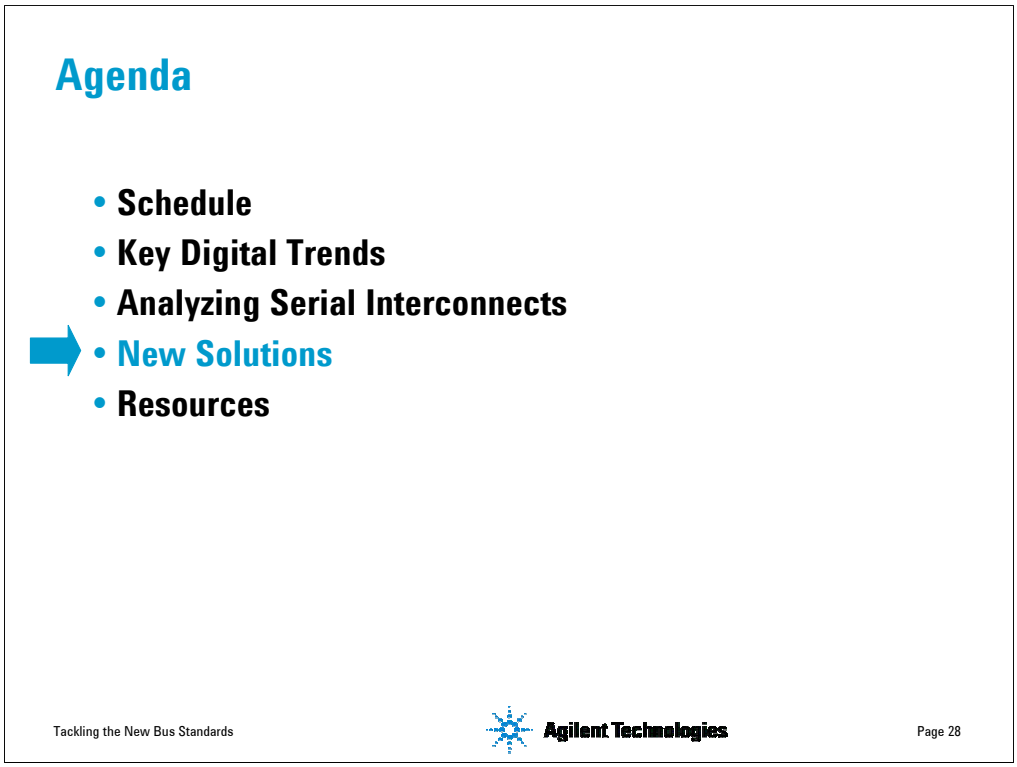
N5393A PCI Express Electrical Compliance & Validation Software



Vendors are required to do all of the tests called for in the bus standard specification. For PCI Express, the Agilent N5393A Compliance and validation test suite is a structured, automated measurement application that performs many more additional tests compared to SigTest. Used in conjunction with the E2688A High-Speed Serial Data Analysis application, the N5393A forms a powerful debug tool for identifying and fixing compliance failures.



In addition, the N5393A provides a marginal analysis to show you just how close you are passing a given spec. This is important to help you to show how much margin is in your system and where your system is most sensitive.

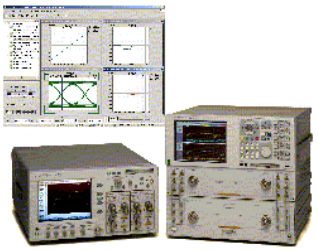


Now let's review the new Agilent solutions and some key digital resources.

Physical Layer Test System Version 2.5

NEW

- 4 Port De-embedding for accurate fixture removal
- Support for VNA (PNA & PNA-L) and DCA/TDR
- Uncoupled start and step settings enable flexible frequency resolution
- Improved data and marker display performance for faster analysis
- View fitted RLCG data display for RLCG model for model confidence check
- Use RLCG W-element smoothing to improve model accuracy using W-element Tabular export
- PRBS bit-pattern in PLTS software to simulate eye-diagrams for pre-compliance testing

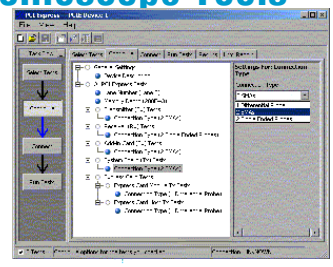


86100C DCA-J/TDR PNA VNA

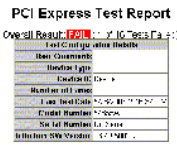
The PLTS system was revised early in 2004 to version 2.5 software. Key enhancements are the support for both VNAs and TDR scopes as measurement platforms. Now you can select the platform that meets your accuracy and modeling needs. Several usability improvement have also been made that make PLTS a much easier tool for the first time user.

Infiniium 54850 Series Oscilloscope Tools

NEW



- **54855A Opt. 008 7 GHz Enhanced BW**
- **N5393A PCI Express Electrical Compliance & Validation Software**
  - E2688A High-Speed Serial Data Analysis
- **N5392A Ethernet Electrical Compliance & Validation Software**
  - 10Base-T, 100Base-TX, 1000Base-T
  - N5395A Ethernet Test Fixture
  - N5396A Gigabit Ethernet Jitter Test Cable
- **N5394A DVI Express Electrical Compliance & Validation Software**



The 54850 Series Infiniium real-time scopes have several new tools aimed at measuring the new serial standards. Option 008 extends the analog bandwidth from 6 GHz to 7 GHz. Three new compliance/analysis software tools address PCI Express, Ethernet and DVI. These tools share a common user interface, are easy to use and automate the complicated test setups plus provide excellent test reports.

86100C DCA-J Adv. Waveform Analysis Software

NEW

Option 201

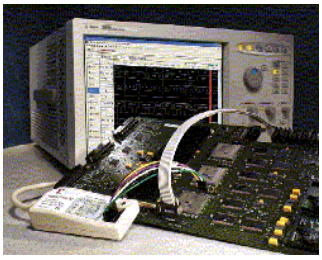
- **Jitter Mode and PatternLock capability with 86107A Precision Timebase Module**
- **Bathtub curve display**
- **Adjustable probability level for Total Jitter (TJ) measurement**
- **Jitter frequency extraction**
- **Sub-Rate Jitter (SRJ) analysis**
- **Long single valued waveform collection**
- **Equalization tool**
- **Requires Options 001 (Trigger) and 200 (Jitter Meas.)**

The 86100C DCA-J was introduced in early 2004 offering significant improvements in the high-speed trigger circuitry, pattern lock, and jitter measurements and decomposition. The new Option 101 extends this capability with some natural refinements such as support for the 86107A precision timebase, for the most accurate, low jitter measurements. The new Equalization tool is very helpful for the next generation high-speed designs by allowing you to have the DCA-J implement an equalization algorithm to see how the measured signal improves/changes.

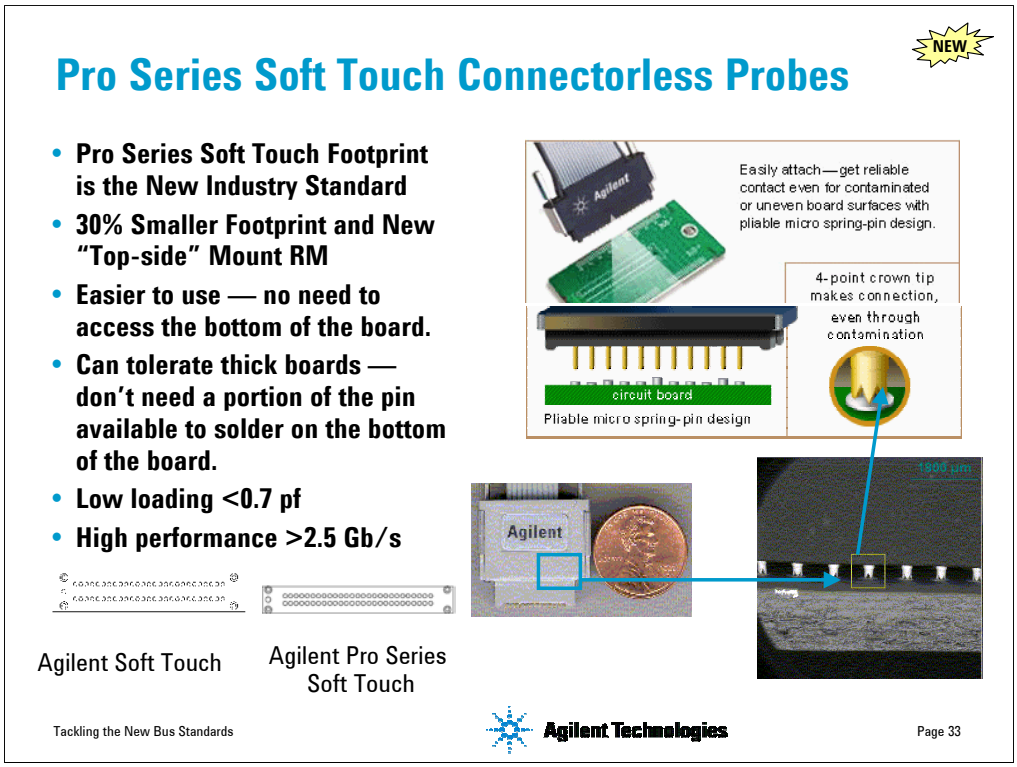
16900 Logic Analysis System

NEW

- **B4655A FPGA Dynamic Probe for Xilinx FPGA debug**
  - Up to 64 internal probe points
  - Measure different groups of signals without recompiling
  - Map internal signal and bus names to the logic analyzer
- **Up to 800 Mb/s data rate measurement modules (16911/50)**
- **Soft Touch Connectorless Probe now an industry standard as "Pro Series"**
- **State-of-the-Art Performance and Usability**
- **World's Only Hosted Modular Logic Analyzer**



The new 16900 Logic Analysis system was introduced in March 2004, offering a significant improvement in logic analysis. In addition to new mainframes and measurement modules, the system features the new B4655A FPGA Dynamic Probe that provides great insight into the timing of Xilinx FPGAs. The Soft Touch connectorless are higher in performance, easier to add to your designs, and now an industry standard.



Recently the industry standardized on a variation of the Agilent Soft Touch probing system – the Pro Series so that users can use the technology and be vendor independent. The Pro Series are 30% smaller in footprint than the original, but retain the same mechanical and electrical design – an endorsement of the quality of these probes and how valuable customers found them.

Soft Touch probes employ micro spring pin technology that is used in very demanding test environments to make a reliable, high-density, and high-integrity connection to signals under test. These micro spring pins mate to a "footprint" of tiny pads (show example) that are laid down on the surface of the board by the designer. The compliance of the pins compensates for variations in the planarity of the board, and the combinations of the spring action and 4-point crown tip on each pin provides a wiping action that clears fine layers of contamination that may be present on the pads. A plastic retention module that is soldered to the board using four small through-holes provides the necessary mechanical alignment and retention.

This approach yields a probing system that is very simple to use, reliable, and very unobtrusive in terms of its electrical and mechanical characteristics. The probe loading is less than 0.7pF, and the footprint is designed to allow for flow-through signal routing so stubs are eliminated – perfect for very high speed signals found in many of today's leading edge designs. We are seeing strong adoption of this probing system, even by designers who don't yet need the very high performance provided by Soft Touch, mostly because of its reliability and simplicity (not having to load a connector).

Soft Touch probes are available in single-ended or differential versions that support all Agilent (and HP) logic analyzers ever manufactured.

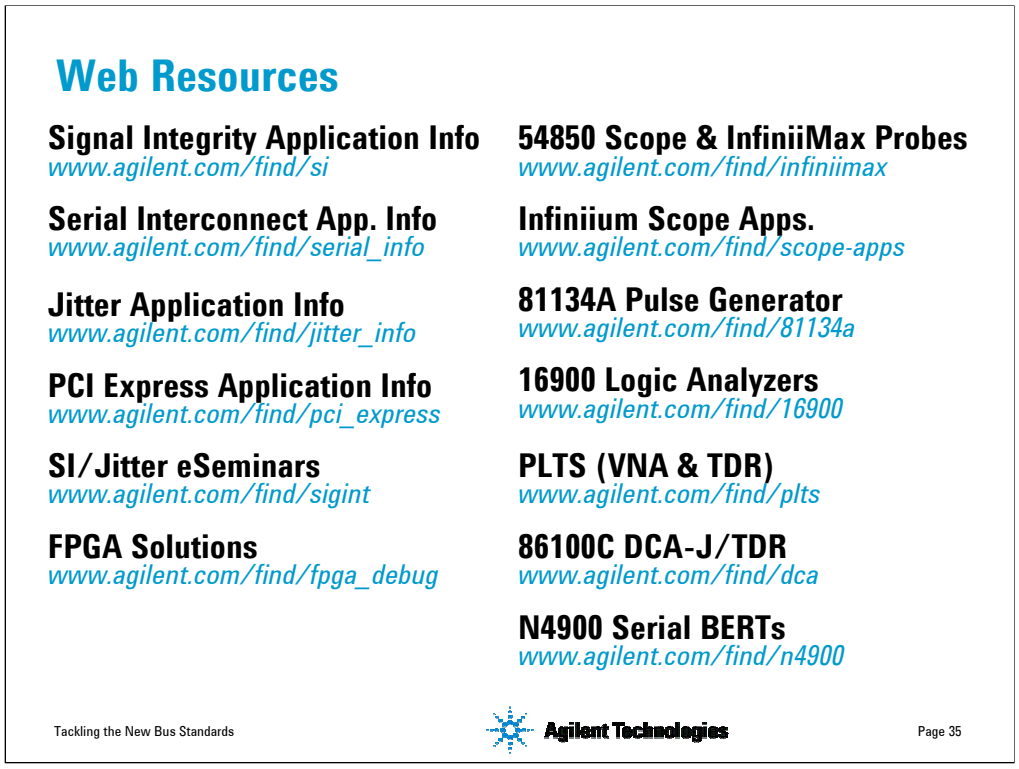
Logic Analysis PCI Express, SATA-II and SAS

NEW

- **N4220B PCI Express Packet Analysis Probe**
  - Data deskew
  - Dedicated hardware packet recognition
  - 4 Programmable packet recognizers per direction of traffic
  - Notification back to logic analyzer
- **N4219B Packet analysis probe for SATA-I/II and SAS**
  - Dedicated packet triggering with 56 bytes of packet header/data
  - Supports 1.5 Gb/s and 3.0 Gb/s
  - Interposer attach snoops bus, allows true in-target testing
  - Supports SSC & OOB

The N4219B is what we call a packet analysis probe. What this means is that it is designed to specifically work in the serial/packetized world. It has built-in packet triggering (we'll explain more about this later in the slideset) that provides triggering on up to 24 bytes of the packet header/data. It supports both 1.5Gb/s and 3.0Gb/s, with auto detect that allows it to follow the SATA bus as it moves from Gen 1 speeds to Gen 2 speeds. It also uses an interposer that allows us to snoop the bus (versus a retiming/repeater) and it allows for true in target testing. This is nice, because the customer can use their own standard SATA cables, etc. without adding a long SATA cable between the probe and the DUT (most competitors require a SATA cable to come out to their box and then another serial ATA cable to go back into the box, often times violating the cable length spec). Our probe has also been designed to work with every Wintel platform logic analyzer we offer, from the 6-slot mainframe (16900/2A), to the 3-slot (16903A) to the benchtops (even the hosted).

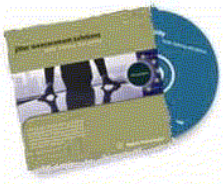
The analysis probe also supports SSC and OOB – both of these are critical capabilities that customers need to have the analysis probe work with. The N4219B supports both SATA and SAS. No need for two separate analysis probes. In addition to supporting both protocols, the N4219B has two ports built into it. This allows it to look at two, full speed, bi-directional links at one time. This will require additional channels. Please note that two bi-directional links cannot be viewed with a stand alone analyzer (like the 1680A). The reason for this is that even though there are enough channels (136 is enough for two, bi-directional links), we can't split 136 channels into four separate machines (we can split it into two).



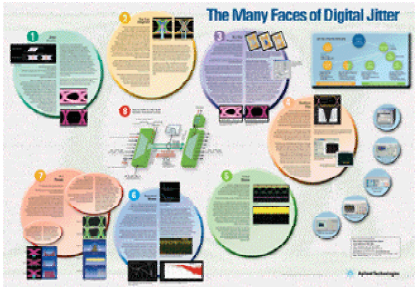
Here are some URLs for the key products and applications.

Signal Integrity & Jitter Tools

SI Solutions CD
(Lit# 5988-6915EN)



Jitter Solutions CD
(Lit# 5988-9350EN)



Jitter Poster
(Lit# 5989-0830EN)

For Signal Integrity and Jitter we have several key tools. There is the Signal Integrity solutions CD. It includes some key eSeminars, data sheets, app. notes, and some demos. There is also a Jitter solutions CD. Just completed in early April 2004 is the "Many Faces of Digital Jitter" poster. It reviews the main jitter measurement viewpoints like eye diagram, bathtub curve, RJ/DJ separation, and more.